Fri, 14 Apr 2006, 5:18:53 PM EST

Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

[redacted]

Recent Search Queries

		Results
#1	((fpga asic pld epld cpld)<in>metadata)	0
#2	((fpga or asic or pld or epld or cpld)<in>metadata)	13087
#3	((((fpga or asic or pld or epld or cpld)<in>metadata))<AND>(test or verification<in>metadata))	5635
#4	((((((fpga or asic or pld or epld or cpld)<in>metadata))<and>(test or verification<in>metadata)))<AND>(datastructure or data-structure<in>metadata))	27
#5	((((((fpga or asic or pld or epld or cpld)<in>metadata))<and>(test or verification<in>metadata)))<AND>(register and (properties or property)<in>metadata))	66
#6	(((((((fpga or asic or pld or epld or cpld)<in>metadata))<and>(test or verification<in>metadata)))<and>(register and (properties or property)<in>metadata)))<AND>(memory<in>metadata))	8

[redacted]

Searching for **(fpga asic pld epld cpld) and test**.
Restrict to: Header No restrictions Order by: Expected citations Hubs Usage Date Try: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP
Results restricted to the title field. **No documents match Boolean query. Trying non-Boolean relevance query.**
Processing 500 documents.
7 documents found. **Order: relevance to query.**

Exploration Bonuses and Dual Control - Dayan, Sejnowski (1996) (12 citations)
exploration bonus. The Maze Case The algorithm was **test**ed on a variety of two dimensional maze tasks
exploration depends on the parameters OE and .We **test**ed the algorithm on three sorts of mazes, two
in the graphs in figure 3. b) The zig-zag maze. We **test**ed how often the agent attempts to go South at A,
ftp.cs.toronto.edu/pub/dayan/exp.ps.Z

Exploration in the Experiment Space: The Relationship between .. - Susan Trickett
has investigated the use of explicit, hypothesis-**test**ing strategies. However, there is evidence that
new hypotheses by searching memory. They stated and **test**ed hypotheses more frequently than participants who
reasoning has focused on explicit hypothesis-**test**ing strategies and is thus associated with
www.aic.nrl.navy.mil/~trafton/papers/Explorations-ExperimentSpace.ps

Synthesis and Simulation of Digital Systems.. - Gupta, Coelho, Jr.. (1992) (55 citations)
programs, a major reason for building dedicated **ASIC** hardware is satisfaction of performance
System for Digital Design,IEEE Design and **Test** Magazine, pp. 37-53, Oct. 1990. 2] J. Rabaey, H.
akebono.stanford.edu/users/coelho/papers/dac-92.ps.gz

An FPGA/FPAA-Based Rapid Prototyping Environment for Mixed.. - Ganesan, Vemuri (1999)
An **FPGA**/FPAA-Based Rapid Prototyping Environment for Mixed
constraint transformation. It involves selection of **ASIC** components from the library and propagation of
the hardware can be performed and the system can be **test**ed in its target environment before hardware
www.ece.uc.edu/~ddel/publications/ganesan-spie-99.ps

Designing a Video Rate Edge Detection ASIC - Mehdi Fesharaki
1993 Designing a Video Rate Edge Detection **ASIC** Mehdi N. Fesharaki and Graham R. Hellestrand
image into regions based on the Kolmogorov-Smirnov **test** is presented. By applying this **test** and comparing
test is presented. By applying this **test** and comparing cumulative distribution functions of
ftp.cse.unsw.edu.au/pub/doc/papers/UNSW/9318.ps.Z

Techniques for Functional Test Pattern Execution - On (1997)
of application specific integrated circuits (**ASICs**) has been recognized as a very labor-intensive
Techniques for Functional **Test** Pattern Execution Abstract Functional debugging
be logically divided into five phases: functional **test** generation, functional **test** execution, error
ftp.cs.ucla.edu/tech-report/97-reports/970025.ps.Z

The e/γ and π/hadron Processor System.. - Perera, Edwards..
technologies we have studied, ranging from **ASIC** design, through high-density packaging, to
operated in the demanding environment of the ATLAS **test**-beam at CERN, and fed with signals from prototype
at 800 Mbaud both in the lab and in the CERN **test**-beam environment. Using a purpose-built real-time
sunset.roma1.infn.it/LEB98/proceedings/perera.ps